REMARKS/ARGUMENTS

The above-identified patent application has been reviewed in light of the Examiner's Action dated June 22, 2007. Claims 10-19 have been canceled in order to expedite prosecution of claims 1-9. However, Applicants expressly reserve the right to pursue the subject matter corresponding to such claims in a divisional application. Accordingly, Claims 1-9 are currently pending.

Applicants would like to thank the Examiner for the courtesies extended during a telephonic interview on September 20, 2007. During the interview, the Examiner and Applicants' representatives, Bradley Knepper and Matthew Ellsworth, discussed the prior art, primarily U.S. Patent Publication No. 2002/0091828 to Kitamura et al. (Hereinafter "Kitamura") in view of the currently pending claims. Applicants' representatives pointed out some differences between the structure of the claimed invention and that of Kitamura. Although no agreement was reached as to any allowable subject matter, the Examiner indicated that she would reconsider Kitamura and whether or not it can be applied to the claimed invention. The Examiner also indicated that if Kitamura cannot be properly applied against the currently pending claims then a new non-final office action would be prepared.

Claims 1-9 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitamura in view of U.S. Patent No. 6,687,797 to Walton et al. (hereinafter "Walton"). In order for a rejection under 35 U.S.C. §103(a) to be proper, the prior art reference or references must teach or suggest all of the claim limitations either expressly or inherently. (MPEP §2143). However, all of the claim limitations set forth in the pending claims cannot be found in Kitmura or Walton. Accordingly, reconsideration and withdrawal of the rejections of the claims are respectfully requested.

The Kitamura reference is directed toward a network storage system that is adapted to be connected between a host computer and a storage device. Data can be sent from a host to a storage device via an interface 12 and fibre channel switch 8. The fibre channel switch 8 depicted in Fig. 18 of Kitamura comprises a network interface 82 and a plurality of ports 81. The fibre channel switch 8 can perform switching operations to complete connections between the

ports 81 of that switch to realize data transfer from a host to channel processors 23' connected thereto.

The storage device subsystem 2' of Kitamura has an intercontroller connecting mechanism 27 that can interconnect a plurality of clusters 26 having a channel processor 23', a drive processor 22', and a plurality of disk units 21 (*i.e.*, storage devices). Data transfer from the host to the storage device always passes through the fibre channel switch 8 to the channel processor 23' where it is stored in a corresponding drive processor 22'. This particular storage system configuration is used to facilitate setting and assigning storage devices to host computers such that each of the host computers can use any one of the storage devices, if necessary. The use of a management means is described to help coordinate these efforts. Kitamura does not teach, suggest, or describe the use of a passive backplane having a plurality of data buses including first and second data buses.

The Walton reference is cited to show that the general use of passive backplanes is well known in the art. The passive backplane in Walton has no active electronic circuitry mounted on or in it and just acts as a passive communications medium. The passive backplane is described as being comprised of one or more substantially planar substrate layers. The substrate layers may be conductive with various pin-and-socket type connectors mounted on it to allow a communication path to other devices connected thereto.

Applicants do not deny that passive backplanes are well known in the art and do not deny that Walton teaches such a passive backplane. However, Applicants respectfully submit that the passive backplane and the interconnection of that passive backplane to various interconnected components as claimed is different from the prior art. More specifically, it is one unique aspect of the present invention that a modular redundant storage subsystem can be created by separating an interface-specific portion (CIMs) from an interface-independent portion (CMMs), which components are interconnected through a passive backplane having a specific bus routing to allow for redundant operation and module failover. The presence or absence of a passive backplane is not what facilitates this redundant storage subsystem. Rather, the passive backplane must have a certain configuration between CIM and CMM modules and contact the right data buses in order to provide features described in the application as filed. Accordingly, it is the

Applicants' view that while Walton generally teaches a passive backplane, Walton does not overcome the shortcomings of Kitamura in meeting the claimed elements related to the passive backplane, and therefore any rejection of the claims over Kitamura in view of Walton should be reconsidered and withdrawn. In particular, replacing the fibre channel switch of Kitamura with the backplane of Walton does not result in the claimed invention.

More specifically, and with respect to claim 1, the Office Action proposes that the signal lines between the I/F 12 and ports 81 as shown in Fig. 18 of Kitamura are equivalent to the at least first and second CIMs claimed in claim 1. Applicants respectfully disagree with this assertion. A port 81 of Kitamura is only shown as being connected to either the I/F 12 of the host computer or a port 231 of a channel processor 23. Moreover, the ports 81 of Kitamura are shown within a network interface 82, and therefore appear to only act as part of a data bus. Similarly, the lines connecting the I/F 12 and the port 81 appear to be nothing more than a bus or signal line for transferring data from the I/F 12 to the port 81. These ports 81 appear to be passive elements that are only responsive to other elements having an operational send or receive data capability.

Claim 1, on the other hand, specifies that each of the first and second CIMs is connected to the passive backplane, the host computer, and the at least one storage device. As noted above, the ports 81 of Kitamura appear to only be connected to an I/F 12 of a host computer or a port 231 of a channel processor 23. Accordingly, there is no connection with a storage device. Additionally, the signal lines between the I/F 12 and the ports 81 of Kitamura cited in the Office Action as corresponding to the claimed CIMs do not have the capability to selectively transfer the storage data to one or more of the plurality of data buses in the passive backplane. Indeed, there is absolutely no teaching, suggestion or disclosure in Kitamura of the lines connecting the 1/F 12 to the port 81 being capable of acting to selectively transfer data. Instead, those lines are simple contacts or connections, not active modules as claimed. In addition, as the Office Action admits, Kitamura does not teach a passive backplane. Moreover, there is no plurality of data buses. The signal lines between the I/Fs 12 and the ports 81 included in the fibre channel switch 8 of Kitamura should not be construed as being able to transfer data to various data buses in a passive backplane nor should such a limitation be obvious in light of Kitamura. For all of these reasons,

Claim 1 is not obvious, and the rejection of Claim 1 and the Claims dependent therefrom should be reconsidered and withdrawn.

With respect to claim 2, the structure of the CIM is further defined to include a communication path portion and a channel interface portion. The communication path portion is operable to selectively transfer storage data between the channel interface portion and the passive backplane. Additionally, the channel interface portion is operable to transfer storage data between the host and/or the storage device and the communication path portion. The Office Action asserts that the I/F 12 equates to the communication path portion as it can control all data transfers on the link between the host and port 81. The Office Action has already described the element between the I/F 12 and the port 81 to be the CIM. The Office Action does not appear to find an element in Kitamura that corresponds to the required channel interface portion that is operable to transfer storage data between the host and/or the storage device and communication path portion. Accordingly, it is requested that the rejection of claim 2 be reconsidered and withdrawn.

With respect to claim 3, a CMM is described that includes a bus interface portion that connects to the passive backplane, a memory for temporary storage of said storage data, and a processing portion that organizes and arranges said storage data. As noted above, the Office Action equates the channel processor 23' to the CMM of the claimed invention. The channel processor 23' is only depicted as including a port 231' for connecting to the network interface 82. Applicants submit that the channel processor 23' of Kitamura does not include either a memory for temporary storage of storage data or a processing portion that organizes and arranges said storage data. Accordingly, it is requested that the rejection of claim 3 be reconsidered and withdrawn.

With respect to claim 4, the bus interface portion of the CMM is further defined. Additionally, a processing interface, bridge core, memory interface, and backplane interface, and an XOR engine and/or DMA engine are provided. The Office Action appears to only find support in Walton for a DMA engine but fails to show that the CMM includes a backplane interface, a memory interface, a processing interface, and a bridge core. Additionally, Applicants fail to see how the combination of the DMA engine discussed in Walton can be combined with

the channel processor 23' of Kitamura to render claim 4 obvious. The fact that a DMA engine is known in the data storage art does not make it obvious to provide a CMM that includes an XOR engine and/or DMA engine. Moreover, the functionality of the DMA controller 408 in Walton is only cursorily described and does not enable one skilled in the art to envision a CMM having a DMA engine that provides DMA access to passive backplane. Accordingly, Applicants respectfully submit that the rejection of claim 4 should be reconsidered and withdrawn.

With respect to claims 5 and 6, the particular configuration of the passive backplane is further defined. More particularly, Claim 5 recites a passive backplane that additionally includes third and fourth data buses, and Claim 6 recites that the first and second data buses are part of a group of backplane buses that includes PCIX buses. Again, Kitamura fails to teach a passive backplane and Walton only appears to generally teach a passive backplane. The Office Action does not reference where in Walton that a passive backplane is taught that either includes third and fourth data buses or where first and second data buses in the passive backplane are taught to be included as part of a group of backplane buses and the group includes PCIX buses. Accordingly, Applicants respectfully submit that the rejections of claims 5 and 6 should be withdrawn since a prima facie showing of obviousness has not yet been made.

With respect to claims 7-9, the interaction between the CIM, CMM, and various data buses on the passive backplane are described. More particularly, Claim 7 recites that the first and second channel interface modules each include two bus ports that connect the communication path portion to the passive backplane, and that the first and second controller memory modules include bus interfaces that are each connected to a bus of the passive backplane. The Office Action does not specifically address these elements of Claim 7. Moreover, it is believed that such elements cannot be found in the cited references. Therefore, Claim 7 should be allowed. Claim 8 depends from Claim 7, and further recites that the bus ports of the channel interface modules and the bus interfaces of the memory controller modules are interconnected in a particular way. The Office Action does not address the elements of Claim 8. Moreover, the cited references do not teach, suggest or describe the claimed configuration. Therefore, Claim 8 should be allowed for at least this additional reason. Claim 9 depends from Claim 8, and further specifies the configuration of the channel interface modules. The elements recited by Claim 9

are not addressed by the Office Action. In addition, the cited references do not teach, suggest or describe the elements of Claim 9. More particularly, as noted above, Kitamura does not describe a passive backplane. Even if Kitamura were found to teach a CIM and CMM as currently claimed, the fact that Kitamura fails to show the relationship between the CIM, CMM, and the passive backplane causes the rejections of claims 7-9 to appear improper. The teaching of a passive backplane in Walton does not overcome these shortcomings as the relationship between the CIM, CMM, and passive backplane is never actually described in the prior art. Accordingly, Applicants respectfully request that the rejection of claims 7-9 be reconsidered and withdrawn.

In addition, Applicants note that the Office Action appears to be incomplete, because it does address all of the limitations of the pending Claims. For example, the Office Action does not appear to find an element in the prior art that corresponds to the recited channel interface portion that is operable to transfer storage data between the host and/or the storage device and communication path portion; the Office Action does not show that the backplane interface, memory interface, processing interface, and bridge core recited by Claim 4 is present in the prior art; the passive backplane with four data busses recited by Claim 5 is not specifically addressed by the Office Action; and the particular arrangements of components recited in Claims 7-9 are not addressed by the Office Action. Accordingly, because the Office Action appears to be incomplete, the Applicants respectfully request that any subsequent actions address the specific limitations these Claims, and respectfully submit that the next Office Action should be non-final for at least this reason.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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